What is claimed is:

1. A memory cell comprising:
a trench capacitor formed in a substrate;
a shallow transistor trench (STT) formed in the substrate;
a transistor comprising
a first diffusion region, the first diffusion region couples the transistor to the gate,
a second diffusion region, the second diffusion region couples the transistor to a bit line, and
a gate serving as a word line, the gate includes a buried portion and a non-buried portion, wherein the buried portion of the gate occupies the shallow transistor trench.

2. The memory cell of claim 1 wherein a width of the STT is less than a lithographic groundrule.

3. The memory cell of claim 2 wherein a width of the non-buried portion of the gate is greater than the width of the STT.

4. The memory cell of claim 3 wherein the first diffusion region is located in a region of the substrate between the trench capacitor and STT and an interface of the STT and substrate between the first and second diffusion region forms a channel of the transistor.

5. The memory cell of claim 2 wherein a width of the non-buried portion is equal to the lithographic groundrule.

6. The memory cell of claim 5 wherein the first diffusion region is located in a region of the substrate between the trench capacitor and STT and an interface of the STT and substrate between the first and second diffusion region forms a channel of the transistor.

7. The memory cell of claim 2 wherein the first diffusion region is located in a region of the substrate between the trench capacitor and STT and an interface of

the STT and substrate between the first and second diffusion region forms a channel of the transistor.

8. The memory cell of claim 1 wherein the first diffusion region is located in a region of the substrate between the trench capacitor and STT and an interface of the STT and substrate between the first and second diffusion region forms a channel of the transistor.

9. The memory cell of claim 1, 2, 3, 4, 5, 6, 7, or 8 wherein the gate comprises doped polysilicon.

Sub A3

10. The memory cell of claim 9 wherein the gate further comprises a cap layer over the non-buried portion the gate.

11. The memory cell of claim 9 wherein the non-buried portion of the gate further comprises a salicide layer on the polysilicon.

Sub A4

12. The memory cell of claim 11 wherein the gate further comprises a cap layer over the non-buried portion the gate.

13. The memory cell of claim 9 further comprises a dielectric layer on an upper portion of the trench capacitor, the dielectric extending to pass an edge of the trench capacitor to a first edge of the STT.

14. The memory cell of claim 13 wherein the dielectric layer comprises silicon oxide.

15. The memory cell of claim 13 wherein the dielectric layer serves as a self-aligned mask to form the STT.

16. The memory cell of claim 15 wherein the dielectric layer comprises silicon oxide.

17. The memory cell of claim 1, 2, 3, 4, 5, 6, 7, or 8 further comprises a dielectric layer on an upper portion of the trench capacitor, the dielectric extending to pass an edge of the trench capacitor to a first edge of the STT.

18. The memory cell of claim 17 wherein the dielectric layer comprises silicon oxide.

19. The memory cell of claim 17 wherein the dielectric layer serves as a self-aligned mask to form the STT.

20. The memory cell of claim 19 wherein the dielectric layer comprises silicon oxide.